Please amend the subject application as follows:

IN THE CLAIMS:

Please withdraw claims 6-22 and 24 without prejudice.

1. (original) A capacitor comprising:

a lower electrode formed on a semiconductor substrate;

a dielectric film stacked on the lower electrode; and

an upper electrode formed on the dielectric film,

wherein the upper electrode is formed by chemical vapor deposition and physical vapor deposition.

2. (original) The capacitor of claim 1, wherein the upper electrode is made of one selected from the group consisting of titanium nitride, tantalum nitride, tungsten nitride, ruthenium, platinum, iridium, and a combination thereof.

3. (original) The capacitor of claim 1, wherein the upper electrode includes a first upper electrode formed by the chemical vapor deposition and a second upper electrode formed by the physical vapor deposition and the first upper electrode and the second upper electrode are sequentially stacked.

4. (original) The capacitor of claim 1, wherein the upper electrode includes a first upper electrode formed by the physical vapor deposition and a second upper electrode formed by the chemical vapor deposition and the first upper electrode and the second upper electrode are sequentially stacked.

5. (original) The capacitor of claim 1, wherein the capacitor is a concave-type capacitor.

6. (withdrawn) A method for fabricating a capacitor, comprising:

forming a lower electrode on a semiconductor substrate;

forming a dielectric film on the lower electrode; and

forming an upper electrode by chemical vapor deposition and physical vapor deposition.

7. (withdrawn) The method of claim 6, wherein the upper electrode is made of one selected from the group consisting of titanium nitride, tantalum nitride, tungsten nitride, ruthenium, platinum, iridium, and a combination thereof.

8. (withdrawn) The method of claim 6, wherein the step of forming the upper electrode comprises:

forming a first upper electrode by the chemical vapor deposition; and

forming a second upper electrode by the physical vapor deposition.

9. (withdrawn) The method of claim 6, wherein the step of forming the upper electrode comprises:

forming a first upper electrode by the physical vapor deposition; and

forming a second upper electrode by the chemical vapor deposition.

10. (withdrawn) The method of claim 9, wherein when the first upper electrode is formed by the physical vapor deposition, a bias power is applied only to a target.

11. (withdrawn) The method of claim 9, wherein when the first upper electrode is formed by the physical vapor deposition, no bias power is applied to the semiconductor substrate.

12. (withdrawn) A method for fabricating a capacitor, comprising:

forming an interlayer dielectric on a semiconductor substrate where a conductive region is formed;

selectively etching the interlayer dielectric to form a concave hole exposing the conductive region;

forming a lower electrode conductive layer in the concave hole and on the interlayer dielectric;

patterning the lower electrode conductive layer to form a lower electrode pattern on a bottom and a sidewall of the concave hole;

forming a dielectric film on the lower electrode pattern;

forming a first upper electrode on the dielectric film by physical vapor deposition; and

forming a second upper electrode on the first upper electrode.

13. (withdrawn) The method of claim 12, wherein when the first upper

electrode is formed by the physical vapor deposition, a bias power is applied only to a target.

14. (withdrawn) The method of claim 12, wherein when the first upper electrode is formed by the physical vapor deposition, no bias power is applied to the semiconductor substrate.

15. (withdrawn) The method of claim 12, wherein the second upper electrode is formed by one of chemical vapor deposition and atomic layer deposition.

16. (withdrawn) A method for fabricating a semiconductor device, comprising:

forming a first interlayer dielectric on a substrate including a transistor;

forming a first opening to expose a drain region of the transistor through the first interlayer dielectric and a second opening to expose a source region of the transistor through the first interlayer dielectric;

filling the first opening and the second opening with a conductive material to form a first contact and a second contact;

forming a second interlayer dielectric on the first interlayer dielectric including the first and second contacts;

forming a concave hole to expose the first contact through the second interlayer dielectric;

forming a lower electrode conductive layer in the concave hole and on the

second interlayer dielectric;

patterning the lower electrode conductive layer to form a lower electrode on a bottom and a sidewall of the concave hole;

forming a dielectric film on the lower electrode; and

forming an upper electrode on the dielectric film by physical vapor deposition and chemical vapor deposition.

17. (withdrawn) The method of claim 16, further comprising:

forming a third interlayer dielectric on the second interlayer dielectric;

forming a third opening to expose the upper electrode through the third interlayer dielectric and a fourth opening to expose the second contact; and

filling the third opening and the fourth opening with a conductive material to form a third contact and a fourth contact.

18. (withdrawn) The method of claim 16, wherein the step of forming the upper electrode comprises:

forming a first upper electrode by the chemical vapor deposition; and

forming a second upper electrode by the physical vapor deposition.

19. (withdrawn) The method of claim 16, wherein the step of forming the upper electrode comprises:

forming a first upper electrode by the physical vapor deposition; and

forming a second upper electrode by the chemical vapor deposition.

20. (withdrawn) The method of claim 19, wherein when the first upper electrode is formed by the physical vapor deposition, a bias power is applied only to a target.

21. (withdrawn) The method of claim 19, wherein when the first upper electrode is formed by the physical vapor deposition, no bias power is applied to the substrate.

22. (withdrawn) The method of claim 16, wherein the lower electrode is cylindrical.

23. (original) A capacitor comprising:

a lower electrode formed on a semiconductor substrate;

a dielectric film stacked on the lower electrode; and

an upper electrode formed on the dielectric film,

wherein the upper electrode is formed by physical vapor deposition and one of chemical vapor deposition and atomic layer deposition.

24. (withdrawn) A method for fabricating a capacitor, comprising:

forming a lower electrode on a semiconductor substrate;

forming a dielectric film on the lower electrode; and

forming an upper electrode by physical vapor deposition and one of chemical

vapor deposition and atomic layer deposition.